European Cooperation in Science and Technology
- COST -
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Secretariat

Brussels, 4 July 2012

COST 4133/12

MEMORANDUM OF UNDERSTANDING

Subject :	Memorandum of Understanding for the implementation of a European Concerted Research Action designated as COST Action IC1202: Timing Analysis on Code-Level (TACLe)

Delegations will find attached the Memorandum of Understanding for COST Action as approved by the COST Committee of Senior Officials (CSO) at its 185th meeting on 6 June 2012.

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MEMORANDUM OF UNDERSTANDING
For the implementation of a European Concerted Research Action designated as

COST Action IC1202
TIMING ANALYSIS ON CODE-LEVEL (TACLe)

The Parties to this Memorandum of Understanding, declaring their common intention to participate in the concerted Action referred to above and described in the technical Annex to the Memorandum, have reached the following understanding:

1. The Action will be carried out in accordance with the provisions of document COST 4154/11 "Rules and Procedures for Implementing COST Actions", or in any new document amending or replacing it, the contents of which the Parties are fully aware of.

2. The main objective of the Action is to develop industrial strength code-level timing analysis techniques for future generation embedded systems.

3. The economic dimension of the activities carried out under the Action has been estimated, on the basis of information available during the planning of the Action, at EUR 40 million in 2012 prices.

4. The Memorandum of Understanding will take effect on being accepted by at least five Parties.

5. The Memorandum of Understanding will remain in force for a period of 4 years, calculated from the date of the first meeting of the Management Committee, unless the duration of the Action is modified according to the provisions of Chapter V of the document referred to in Point 1 above.

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A. ABSTRACT AND KEYWORDS

Embedded systems increasingly permeate our daily lives. Many of those systems are business- or safety-critical, with strict timing requirements. Code-level timing analysis (used to analyse software running on some given hardware w.r.t. its timing properties) is an indispensable technique for ascertaining whether or not these requirements are met. However, recent developments in hardware, especially multi-core processors, and in software organisation render analysis increasingly more difficult, thus challenging the evolution of timing analysis techniques. New principles for building "timing-composable" embedded systems are needed in order to make timing analysis tractable in the future. This requires improved contacts within the timing analysis community, as well as with related communities dealing with other forms of analysis such as model-checking and type-inference, and with computer architectures and compilers. The goal of this COST Action is to gather these forces in order to develop industrial-strength code-level timing analysis techniques for future-generation embedded systems.

Keywords: real-time systems, WCET analysis, code generation, time-predictable computer architecture, safety-critical embedded systems

B. BACKGROUND

B.1 General background

Embedded systems are digital computing systems that are embedded in a larger product, e.g. an airbag control unit embedded in a car. Many embedded systems are *real-time* systems where firm deadlines for the information-processing must be met. Missing a deadline can have catastrophic consequences, up to the loss of human life. **This Action is focused around analytic techniques and software tools to ensure that such deadlines will be met despite rapidly evolving hardware and software development practices.**

Embedded systems consist of a hardware execution platform and software code running on it. *Code-level timing analysis (CLTA)* estimates the execution time for single *tasks* running on given hardware, whereas *system-level timing analysis* uses these estimates to verify whether deadlines are met. Usually, CLTA determines estimates of the code's *Worst-, Best- or Average-Case Execution Time (WCET, BCET, ACET)*. In particular worst-case timings, derived by a so-called *WCET analysis*, are used to verify deadlines. **This verification is crucial for ensuring the safe functionality of embedded safety-critical systems, and is thus becoming extremely important as such systems increasingly surround us in vehicles, factories, hospitals, and other environments**. The research coordinated by this Action will therefore have a strong focus on CLTA for worst-case timing.

CLTA is well understood for single-core processors. CLTA (especially WCET analysis) for *multi-core* processors is still in its infancy, however, and since these processors are rapidly conquering the market, there is an urgent need to develop CLTA for them. Moreover, the way software is produced is shifting towards component-based and model-driven approaches. This creates new challenges for CLTA as the code to be analysed will have new and different structures and properties.

The research necessary to develop CLTA for these systems is currently fragmented into groups focusing on different technologies, which in turn are parts of larger, mostly disjoint communities. The successful development of CLTA requires communication, coordination, and cooperation between these communities. This Action will provide the required means. The most important scientific achievements to make are: timing analysis for multi-cores; improved hardware/software support for such analyses; and multi-objective approaches additionally considering other important resources, such as energy. The goal of the Action is to promote the development of technology with the reach and power to perform CLTA for industrial-scale hardware and software systems. A COST Action is the best option to achieve this goal, as the research of the relevant European groups in this area is already funded by European research programs and national funding agencies.

B.2 Current state of knowledge

Code-level timing analysis takes two forms: measurement-based analysis and static program analysis. Measurement-based approaches rely on instrumented program executions, whereas static analyses apply formal methods to the code without running it. Static WCET analysis can obtain *provably safe* timing guarantees which is crucial when verifying timing properties of safety-critical systems. Europe is the world leader in WCET analysis, with the most sophisticated commercial and academic WCET analysis tools.

CLTA for worst-case execution time is currently only applicable to single-core processors. For multi-cores, the complex interaction between cores make timing analysis very challenging, and it is a field of active research. One way around the problem is to design multi-cores with less complex timing models. The European Seventh Framework Programme (FP7) project PREDATOR proposed the "PROMPT" design principles for predictable multi-core architectures, minimising simultaneous accesses to shared resources. These design principles are still preliminary, though, and multi-cores abiding to them are still to be seen. Thus, both the furthering of these principles as well as the development of CLTA for current multi-cores will be central to this COST Action.

Static WCET analysis, of particular interest for safety-critical applications, is currently poorly automated. The user often has to provide information ("flow facts") about possible program flows, such as loop iteration bounds. Furthermore, a safe WCET analysis must be applied to the final, linked binary rather than to the source code. Thus, static WCET analysis is currently a tedious and error-prone task that takes place only at the late verification stage of software development. It is highly desirable to have timing estimates early in the design process. For ACET, Source-Level Simulation (SLS) provides a way to obtain such estimates. However, for the dimensioning and time budgeting of safety-critical real-time systems, WCET estimates are much more relevant before crucial design decisions are taken. While SLS may be applied also here, faster and more reliable methods are much needed. For these reasons, CLTA is not yet integral part of most industrial software development processes.

Software timing depends strongly on how the software is written and compiled. Some recent compilers use WCET estimates to optimise for reduced WCET. However, these compilers currently only optimise code for single-core systems. PREDATOR has also proposed coding guidelines to improve the timing analysability of Matlab/Simulink models, but these rules are sufficiently restrictive that they are not feasible in practice. A further hindrance for broad industrial CLTA use is the poor integration of the various tools. Software development tools mostly use native interfaces, without any established inter-tool interface standards. This complicates the integration of timing analysis tools into existing tool chains. The EU FP7 project ALL-TIMES has focused on the interoperability of timing analysis tools. However, ALL-TIMES considered only a small number of tools, and common standards for tool inter-operation are still lacking.

Timing is not the only criterion to be considered during system development. Many real-time systems are also constrained e.g., in terms of energy or code size. However, researchers have not yet systematically investigated this trade-off between different design goals. The only published approach to date involves reorganising WCET-aware compiler optimisations to trade WCET for ACET and code size. Model-checking of priced timed automata may provide an interesting way forward here.

B.3 Reasons for the Action

This Action has been launched in response to the current fragmentation of research in code-level timing analysis. Many groups are working in isolation, and none has the critical mass to tackle the challenge of new multi-core architectures by itself. A coordinated effort is needed to integrate tools, develop new approaches for next-generation multi-cores, and develop new early-stage timing analyses.

The Action meets both scientific *and* economic needs. Scientifically, multi-cores impose a major challenge to CLTA, and techniques for accurate/fast early-stage timing analysis are also demanding. Economically, CLTA for multi-cores will be much needed to support the development of safety-critical embedded systems, reducing development costs as well as the risk of system failure. Better ways to design embedded systems will also save natural resources such as energy, and thus improve sustainability.

By coordinating and reinforcing research in CLTA, this Action will focus attention on technology that has far greater reach and power, and that can be applied to realistic, industrial real-time software running on next-generation multi-core hardware. The new technologies will benefit Europe's world-leading manufacturers, e.g., in automotive, avionics or telecommunication. The successful implementation of the Action will contribute to maintaining Europe's leading role in the field of CLTA, thus providing European tool providers the chance to conquer top positions on the software-development tool market in the growing segment of safety-critical real-time applications.

B.4 Complementarity with other research programmes

The Action complements research activities in the following European programmes: **EU Framework 7**, Objective 3.3 (Embedded Systems, provides general support for collaborative projects that use or develop CLTA); **ARTEMIS-JU** (supports industrially-based collaborative projects in the general field of embedded systems that may use CLTA). **Horizon 2020** is expected to follow a similar pattern, but will no longer support large-scale Networks of Excellence which could compete with this Action. Although the above programmes may exploit CLTA results and technologies and support specific focused research activities, they do not provide the coordinated focus on CLTA that would be offered by the Action, or generally provide the critical mass of networking/coordination that is needed to ensure joined-up progress on the Action's objectives.

The Action complements the following European projects, all of which have a strong complement of researchers who have been involved in preparing this Action:

- parMERASA (Multi-Core Execution of Parallelised Hard Real-Time Applications Supporting Analysability, Specific Targeted Research Project (STReP)): focuses on parallelisation of hard real-time applications for multi-cores.
- PROARTIS (Probabilistically Analysable Real-Time Systems, STReP): explores probabilistic techniques for the analysis of the timing behaviour of execution resources at processor and software level.

- HiPEAC (NoE on High Performance and Embedded Architecture and Compilation): concentrates on HW and SW design for embedded high-performance multi-core systems.
- T-CREST (Time-predictable Multi-Core Architecture for Embedded Systems, STReP): focuses on designing timing-predictable multi-cores and on timing analysis and code generation for these.
- RECOMP (Reduced Certification Costs Using Trusted Multi-core Platforms, ARTEMIS): explores the use of multi-cores in safety-critical systems.

parMERASA, PROARTIS, T-CREST and RECOMP are targeted projects with the primary aim to undertake specific research tasks rather than networking and coordination. The Action therefore complements them in providing a focal point for networking and coordination across the entire CLTA community. The Action complements HiPEAC in that timing analysis is not present at all in HiPEAC. No other project aims to bring together the research communities that are key to make the required progress in CLTA.

C. OBJECTIVES AND BENEFITS

C.1 Aim

The main objective of the Action is to develop industrial strength code-level timing analysis techniques for future generation embedded systems.

C.2 Objectives

The secondary objectives of the Action are:

- to develop improved methods for CLTA that can deliver precise timing estimates for multi-core architectures;
- to further develop design principles for hard-/software and systems that improve timing predictability;

- to increase the usability of timing analysis tools through:
  - higher level of automation,
  - better integration of code-level timing analysis in development processes;
- to promote the exchange of ideas with neighbouring research communities in order to:
  - enhance timing analysis by incorporating related analysis techniques,
  - extend timing analysis techniques to other resources than time;
- to enhance coordination and interaction between European researchers and tool vendors in the field of CLTA;
- to influence the development of future multi-core architectures for real-time embedded systems so that CLTA requirements are considered as an integral part of the hardware design process.

C.3 How networking within the Action will yield the objectives?

In order to successfully undertake and bring to completion the range of activities coordinated by this Action, expertise is needed in several complementary areas: formal methods; code-level analysis; multi-core architectures; industrial practices, needs and requirements; software tool implementation; benchmarking.

No single research group, company or institution alone possesses this full breadth of expertise. The required expertise is distributed across a large number of European and non-European research groups who are only in irregular contact. The Action will collate this dispersed expertise, bringing it to bear on a common set of objectives, deploying efficient, low-overhead coordination that will be concentrated on facilitating the dissemination of problems, solutions, ideas and proposals across research partners and helping them mature. The Action will deploy this expertise through the following Working Groups (WGs), each dealing with a single focused set of issues:

- WG1: Timing models for multi-cores and timing composability;
- WG2: Tooling aspects;
- WG3: Early-stage timing analysis;
- WG4: Resources other than time.

The Action will promote a regular series of research visits and exchanges, presentations, demonstration and discussion events and workshops that will allow expertise to be shared among participants. Visits will involve both early-stage and experienced researchers. The Action will also directly promote exchanges and visits between industrial and academic participants, including the incorporation of industrial placements for suitably qualified undergraduate and postgraduate students.

C.4 Potential impact of the Action

This Action has clear potential for significant impact in both **scientific** and **economic/societal** terms. Tangible and quantifiable scientific results include:

1. producing new (formal) models of **multi-core timing behaviour**;
2. providing **provable guarantees** of multi-core timing behaviour;
3. **advancing compilation for real-time systems** towards multi-task and multi-core systems;
4. **focusing European research effort** on containing the cost and risk of developing time-critical applications on multi-core systems.

Economic/societal benefits include:

1. **furthering the European lead** in tools for analysing timing behaviour;
2. facilitating the **development of new commercial tools** for analysing multi-core timing behaviour;
3. increasing the **market penetration** of state-of-the-art timing analysis in the embedded systems industry, with consequent **improvement in safety guarantees** for the consumer;
4. further promoting European excellence in and providing opportunities for **highly-skilled employment** in the development of safety-critical systems.

C.5 Target groups/end users

The target groups for the Action are academic and industrial researchers in: safety-critical systems; formal methods; computer architecture; embedded systems; compilation; timing cost models and analyses; worst-case execution time analysis; benchmarking. Researchers from all the aforementioned disciplines have participated in the preparation of the Action.

The Action targets companies with expertise in: tools for WCET analysis; compilers and tools for embedded systems design; hardware design and implementation for embedded systems; development of safety-critical systems, including automotive, avionics, energy generation and control engineering. Experts from WCET tool vendors have participated in the preparation of the Action.

The ultimate end-users and beneficiaries of the research will be European and non-European citizens at large, who will benefit from safer, faster, more energy-efficient and thus sustainable real-time embedded systems, including, for example, home automation to support an ageing population, safer, more secure and more efficient transport and housing, improved manufacturing processes, better use of scarce energy resources, and increased levels of skilled employment.

D. SCIENTIFIC PROGRAMME

D.1 Scientific focus

The scientific focus of the Action is on making the key scientific and technical advances that are necessary to ensure widespread use of code-level timing analysis. The following research tasks will be undertaken in order to achieve this:

- modelling the timing behaviour of multi-core platforms, using these models in more precise timing analyses;
- further developing principles for timing-predictable multi-core architectures;
- increasing the level of automation of timing analysis;

- widening the scope of timing analysis from timing verification to early timing estimation;
- adapting techniques for compilation and code generation to aid timing analysis;
- combining techniques for timing analysis with other resource analyses.

The work plan to carry out the research tasks coordinated by the Action can be briefly summarised in the following steps:

- study current and emerging multi-core architectures to understand their timing properties, and identify impediments to timing predictability (WG1);
- apply different analysis approaches to see how to best deal with these impediments in timing analysis (WG1);
- combining knowledge about architectures and analysis techniques, devise improved principles to make multi-core architectures more timing predictable (WG1);
- apply the approach of combined analysis techniques to increase the general usability of tools and techniques (WG2);
- further strengthen these approaches by studying how compilers and code generators can help achieving timing predictability (WG2);
- study early-stage, fast timing analyses to allow fast exploration of alternative hardware (WG3);
- study the interplay between timing analysis and analyses for other resources, in order to strengthen them by cross-pollination (WG4);
- facilitate the work by developing common formats and open benchmark suites (WG2);
- evaluate resulting techniques, tools, and architectural principles on industrial benchmarks (WG2).

D.2 Scientific work plan methods and means

To achieve the objectives of the Action, coordinated research is required in several areas. Each area is the focus of a Working Group, as defined in Section C.3. The scientific work plans of the individual Working Groups are detailed below.

Working Group 1: Timing models for multi-cores and timing composability

Recent advances in computer architecture, in particular the arrival of *multi-core/manycore* processors where hardware resources are shared between processor cores, have introduced major new challenges in timing analysis. On such processors, activities on one core can affect the timing of activities on other cores. It is no longer possible to consider execution times independently for each core: rather, timing analysis must take all possible simultaneous activities into account. These processor architectures thus lack *timing composability*, i.e., the ability to infer the timing for the full system from the timing of its isolated parts. This affects very adversely the *timing predictability* of these systems. The problem is aggravated by increasingly complex software.

A tight interaction between hardware/software designers and timing analysis experts is required to face this new challenge. A key objective for this Working Group is to bring these two communities together, thus increasing the potential for innovation.

This Working Group will take a two-pronged approach to the timing analysis problem. First, the Working Group will work towards hardware designs controlling how threads in multi-cores interact. If successful, this will allow threads to be analysed in isolation, significantly reducing the cost for verification. The focus will be on shared hardware within multi-cores, as this is the main source of time unpredictability and reduced time composability:

- on-chip memory (e.g. cache) contention;
- interconnection networks (bus, network on chip);
- off-chip resources such as external memory.

Second, the Working Group will define analysis methods for current real-time multi-core architectures. A major goal is to understand the current generation of real-time multi-core processors. Different research groups will work together to analyse the latest actual real-time multi-core processors, in order to identify causes of execution time variability. New innovations in analysis techniques are needed to cope with this complexity. The Working Group will also study how system and application software design influences analysability.

The Working Group will:

- define new hardware mechanisms for multi-core platforms that provide both temporal predictability and composability;
- study the predictability of current multi-cores and define new analysis methods.

Working Group 2: Tooling Aspects

Code-level timing analysis can only be industrially successful if it is sufficiently automated, by tools fitting into industrial design flows. This Working Group will perform research supporting these tooling aspects, including associated tools like compilers. Furthermore, it will develop support for the evaluation of tools and methods.

The Working Group will extend WCET-aware compilation to multi-core systems. The approach to this challenge will be to tightly couple the compiler with the operating system and the underlying multi-core system model. In this way, the compiler can run timing analyses that will bound timing interference, and can apply optimisations that reduce the effect of this interference.

Current static timing analysis tools rely on manually-provided constraints on possible program flows. This fact is a hindrance to the industrial uptake. This Working Group will improve the level of automation by sharpening current approaches to automatic program flow analysis. Flow analyses will be combined with techniques from other areas such as model-checking, type-inference and loop-invariant generation. The Working Group will also investigate how to reuse pre-computed analysis results - e.g., from the analysis of libraries.

The timing analysis tools in use today mostly lack common interfaces, particularly for flow-fact specification. This is a hindrance for their integration into tool chains. To remedy this, a common flow-fact description language will be designed. A formal semantics will be provided in order to avoid ambiguity.

Different timing analysis tools need to be evaluated and compared. This WG will periodically pursue an open timing analysis "tool challenge", where CLTA tools will be applied to a common set of realistic, industrially relevant timing analysis problems.

Good, realistic benchmark suites are essential for the evaluation of techniques and tools. Existing benchmark suites for CLTA do not cover multi-core software. The Action will provide a freely available benchmark suite for timing analysis, featuring complex multi-core benchmarks, with the goal of establishing it as the standard benchmark suite for timing analysis.

This Working Group will:

- develop methods for WCET-aware compilation for multi-core systems;
- improve automation by investigating advanced flow analyses;
- unify program flow constraint languages;
- run an international tool challenge, and provide and maintain a publicly available benchmark suite.

Working Group 3: Early-stage timing analysis

WCET analysis has traditionally been used in the verification phase of a system, after all components have been built. Since redesigning a software system is very costly, designers usually choose to over-specify the hardware initially and then just verify that it is indeed sufficiently powerful. However, as systems' complexity rises, these initial safety margins can prove to be very expensive. Undertaking lightweight (but less precise) analysis in the early stages of the design process has the potential to drastically reduce total hardware costs.

A second related issue is that of *portable* WCET analysis. When the early-stage analysis is performed, it is clearly targeted at selecting a platform which is cost-efficient for the problem at hand. It would be highly beneficial to perform the WCET analysis in such a way that *parts of the analysis can be redeployed on other hardware platforms*, in order to avoid ballooning costs in the analysis.

To address this, we will study:

- Methods to derive approximate and/or abstract timing models for source code, for higher-level models from which code can be generated, and the associated timing analysis methods. This may be achieved by:
    - online estimation of parameters like preemption delay, WCET and cache contention; or
    - by model-checking-based approximate timing analysis.
- Methods for fast exploration of hardware alternatives using timing estimates derived from modular, approximate, timing-composable hardware models.

Working Group 4: Other resources than time

For embedded systems design, it is paramount that timing analysis be reconciled with other resource constraints. This is best done within models that permit the exploration of trade-offs between multiple dimensions, such as functionality, performance, quality-of-service and resource consumption. To support compositionality, this ability must be carefully balanced against the need to separate concerns as much as possible. This Working Group aims to find formalisms that are appropriate for different purposes, such as time-energy trade-offs in energy-constrained computing. In order to support component-based design, the relevant dimensions must then, ideally, be captured within interfaces. The timing analysis community has developed sophisticated analysis methods which likely can be adapted to also analyse other resources. This Working Group will interact with the other concerned research communities to achieve this. This Working Group will address:

- Modifying timing analysis techniques to work for resources such as energy dissipation and memory. For energy, this could be achieved by further development of the priced time-automata model and combining techniques from model-checking and static analysis, or by using amortised analysis. Secondly, probabilistic methods will be deployed to gauge the expected spare capacity in the system. The results of both approaches will be exploited into e.g., optimal energy-aware scheduling strategies.

- How analyses for different kinds of resources can support multi-objective optimisation. One line of research for this will involve the continuation of existing work on multi-weighted automata and on multi-weighted modal transition systems with structured labels - allowing for analysis of multi-objective optimisations.
- Multi-objective optimisation during code generation through integration of more detailed energy models for actual processor architectures to WCET-aware compilers and through two-phase optimisations.

E. ORGANISATION

E.1 Coordination and organisation

Management Committee (MC)

The MC will comprise one representative from each participating party, with a single vote each. Decisions will be taken by majority vote. The responsibilities of the MC are:

- planning and coordination of the MC meetings, scientific meetings, as well as workshops;
- periodic review of the different activities (Short-Term Scientific Missions (STSM), publications, training schools, etc.) in order to meet the objectives of the Action;
- interface with the Industrial Advisory Board (IAB);
- progress tracking of each WG against its objectives;
- promotion of collaboration and knowledge/data exchange between partners from different WGs;
- promotion and approval of STSMs in particular for PhD student and junior researcher exchange;
- integration of new partners;
- creation and regular updating of the Action's website;
- coordination and facilitation of effort aimed at the preparation of research project proposals related to the topics of the Action, with the intention of establishing at least one EU Horizon 2020 project.

Meetings of the MC will be linked with WG meetings and an annual workshop on code-level timing analysis. This will ensure the MC is fully engaged with the research community as well as enabling good networking/collaboration opportunities.

External Presentation and Interaction

The MC and WGs will be advised by an *Industrial Advisory Board (IAB)* formed by end-users of the technologies developed in the area of avionics, automotive and industrial electronics. This is designed to ensure that the Action is targeting relevant challenges. The results of the Action will be directly presented via the annual timing analysis workshop and other workshops. In order to facilitate the transfer of academic knowledge into industrial practice, industry will be actively invited to these workshops. This will be complemented by tutorials on tools and techniques, to be co-located with suitable conferences/industrial congresses.

The MC will also maintain a dynamic and visible website as the external face of the Action. This will contain among other things: i) a regularly-updated news section; ii) a list of relevant publications; iii) software prototypes developed in the context of the Action; and iv) training material, as it becomes available from the tutorials.

Training Young Researchers

Training of young researchers will be achieved via two central mechanisms. Firstly, the tutorials are intended to cater for the training of young researchers as well as external researchers and industry. Tutorials will be geared towards broadening the understanding of different techniques and methodologies for code-level timing analysis, encouraging young researchers to engage with existing research. Secondly, STSMs will be mostly deployed to support mobility of students and junior researchers between different sites.

Milestones

Apart from the workshops, milestone dates are given relative to the start month T0 of the Action.

T2	Website operational with presentation of the current activities of the participants (including all mandatory parts)
July 2013/2014/2015/2016	International workshop on code-level timing analysis
T15/T39	Tool Challenge announced including all rules
T24/T48	Reports on Tool Challenge results
T24	Submitted joint research proposal to a suitable EU Horizon 2020 call

E.2 Working Groups

Each WG will be managed by a WG Coordinator. The main tasks of a WG Coordinator are to: plan appropriate scientific meetings for the WG; coordinate activities within their WG in order to meet the objectives that are defined in the scientific programme; promote the set-up of joint research (e.g., making use of STSMs and PhD student exchanges); promote the writing of common scientific and technical publications; report WG progress to the Action Chair and MC; participate in MC meetings.

The WGs will meet twice a year in a single joint event. This frequency is intended to ensure an optimal exchange of ideas, and will be supplemented by telephone conferences as appropriate. Each meeting will comprise a day long (or longer) discussion forum, where the first half of the meeting will be devoted to individual Working Groups, and the second half will be devoted to inter-Working-Group exchange. In order to enhance participation, WG meetings will be held in different host countries. They will be accompanied alternately by open thematic workshops and by the Action's timing analysis workshop, which will complement the managed WG programme and provide opportunities for interaction with researchers who are not Action participants.

E.3 Liaison and interaction with other research programmes

The Action will liaise with the EU FP7 projects mentioned in Section B.4 and with other relevant international and national projects. This interaction will be facilitated by those participants in the Action who also participate in these other projects. Furthermore, key representatives of other research programmes will be invited to participate in selected activities of the Action (meetings, workshops, etc.).

E.4 Gender balance and involvement of early-stage researchers

This COST Action will respect an appropriate gender balance in all its activities and the Management Committee will place this as a standard item on all its MC agendas. The Action will also be committed to considerably involve early-stage researchers. This item will also be placed as a standard item on all MC agendas.

The Action's tutorials for young researchers will build up expertise in code-level timing analysis, help overcome the fragmentation of the field and increase research capacity by encouraging new researchers into code-level timing analysis: young researchers will learn early on in their career about different techniques and methodologies for code-level timing analysis that may be beyond those used in their home institution, and will be encouraged to use these approaches in their own research. Short-term exchanges of young researchers and PhD students between the participating groups will be a central pillar of the Action, as this permits young researchers to develop lasting contacts and extend their research expertise.

The preparation of this Action has already involved several of the leading female researchers in the field. All Action participants will be explicitly encouraged to promote the involvement of female professionals in the various activities, in particular in leadership positions such as WG Coordinators and MC members, and will be required to adhere to gender equality principles when selecting and/or appointing new recruits.

F. TIMETABLE

- The duration of the Action is 4 years.
- The Kick-Off Meeting will start the Action. During the meeting, the WG Coordinators will be appointed.
- The Action's website will be created soon after the Kick-Off Meeting and will be updated continuously.
- Twice a year, meetings of the Management Committee and the Working Groups will take place.
- Annually, a workshop on code-level timing analysis will take place.
- In years two and four of the Action, a timing analysis tool challenge will be organised.
- Short-term Scientific Missions can be requested any time after the Kick-Off Meeting.
- Thematic workshops, tutorials and courses will be organised with an open schedule and according to the needs of the WGs.

The timetable of the Action is summarised in the following diagram:

	Year 1	**Year 1**	**Year 2**	**Year2**	**Year 3**	**Year 3**	**Year 4**	**Year 4**
Coordination	X	X	X	X	X	X	X	X
Kick-Off Meeting	X							
Website	X	X	X	X	X	X	X	X
Reporting		X		X		X		X
MC Meeting	X	X	X	X	X	X	X	X
WG Meetings	X	X	X	X	X	X	X	X
Timing analysis workshop		X		X		X		X
Tool challenge			X				X	

G. ECONOMIC DIMENSION

The following COST countries have actively participated in the preparation of the Action or otherwise indicated their interest: AT, DE, DK, ES, FI, FR, IT, PT, SE, UK. On the basis of national estimates, the economic dimension of the activities to be carried out under the Action has been estimated at 40 Million € for the total duration of the Action. This estimate is valid under the assumption that all the countries mentioned above but no other countries will participate in the Action. Any departure from this will change the total cost accordingly.

H. DISSEMINATION PLAN

H.1 Who?

Target audiences for the dissemination of the results of the Action are:

- the scientific community;
- the software industry (both in Europe and worldwide), specifically timing analysis tool vendors;
- industry manufacturing hard and soft real-time systems (both in Europe and worldwide), i.e., end-users of code-level timing analysis such as automotive, avionics, automation, telecommunication or medical engineering industries, or third-party suppliers;
- students and lecturers in computer science and/or real-time systems;
- the general public.

H.2 What?

The results of the Action will be disseminated in a number of ways, including

- publicly available timing analysis tools, real-time operating systems, processor and network designs, and benchmarks that can be freely downloaded via the Internet;
- refereed scientific publications;
- the Action's website;
- organisation of and participation in meetings, workshops and conferences, tutorials and tool challenges;
- presentations and exhibitions at industrial congresses and trade fairs;
- university-level education;
- technical documents and guidelines;
- a public e-mail mailing list;
- press releases.

H.3 How?

Publicly available software for free download: In order to achieve a broad and direct worldwide dissemination of the Action's achievements, it is foreseen to make software tools for timing analysis and relevant benchmark suites freely available whenever possible. The MC will promote to make software developed within the Action publicly available for free download via the Internet.

Publications: Scientific results of the Action will be disseminated through refereed scientific journals and conference proceedings and through technical documents/white-papers focusing on one or more technical aspects of code-level timing analysis. Joint publications will be encouraged by the MC.

Website: A public website will provide information to the international scientific community, to industry, and to the general public. It will also facilitate communication between participants. The website will combine a public part plus an access-restricted intranet for participants in the Action.

The website will contain, among other things:

- general information about COST and this Action, including its activities (meetings, etc.) and contact information for participants in the Action;
- download links for publicly available software developed by the participants, in particular timing analysis tools and benchmarks;
- relevant publications produced by participants in the Action;
- information for the public and for the industrial target groups;
- on-line proceedings, slides and posters from tutorials, trainings and WG meetings;
- STSM (Short-Term Scientific Missions) calls and reports;
- teaching materials (slides, course notes, labs, etc.);
- links to websites related to timing analysis;
- job announcements.

STSM: STSMs will facilitate scientific networking, technology transfer within and outside the Action, and training in new techniques.

International Conferences and Workshops: The Action's participants will organise scientific as well as industrial workshops/conferences to inform interested scientists and industrial practitioners about the results of the Action and about new technologies developed through the project. These workshops will provide hands-on practical training as well as theoretical information. As a concrete example, it is foreseen that the Action will organise an international workshop on code-level timing analysis on an annual basis as *the* premier event where international experts in timing analysis meet. Knowledge and data resulting from the Action's activities will also be integrated and presented at international conferences. This will promote European know-how and increase international collaboration.

Tutorials: In order to reach a broad audience from both academia and industry, the Action will organise tutorials about recent advances in timing analysis. To strengthen the hands-on character of such tutorials, talks will be linked with tool demonstrations where software developed within the Action is put in the spotlight.

Tool challenges: A timing analysis tool challenge, where partners from the Action but also from outside will have their software tools applied to realistic timing analysis problems, will be organised every two years by the Action.

Teaching activities: University teaching activities at both undergraduate and post-graduate level will take advantage of the knowledge and experience acquired during this COST Action. Young scientists and engineers will be informed and trained in the latest developments in design and analysis of real-time systems.

E-Mail Bulletins: Important results of the Action such as new software versions and announcements of workshops, tutorials or vacant jobs will be disseminated via the Action's international e-mail network.

Press releases: The first press release will be launched in all participating countries in conjunction with the Action's Kick-Off Meeting. Further press releases will inform the general public of important results of the Action.

Depending on progress, this dissemination plan might be adapted in the course of the Action. The MC will regularly monitor and evaluate the results of the Action and update the dissemination plan.