Short Term Scientific Mission Report on Applying Timing Analysis Meta-model to Co-Simulation Model Based Development Environment

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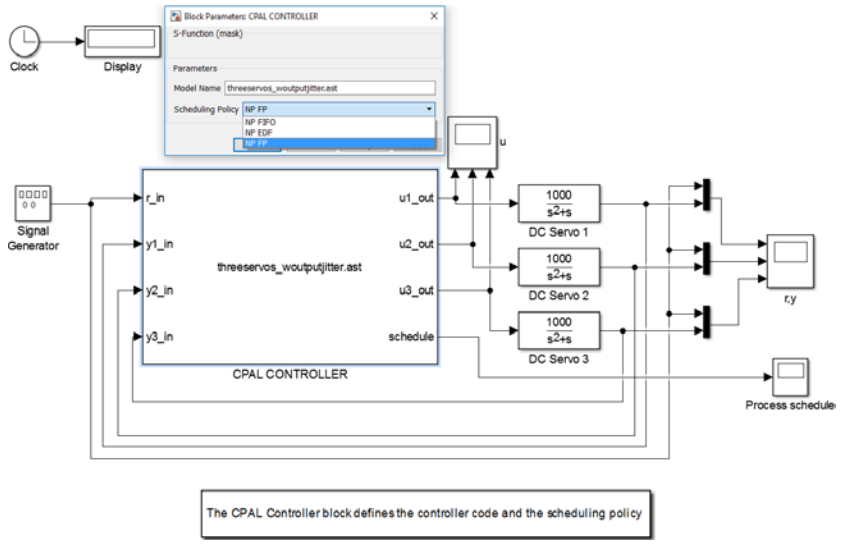
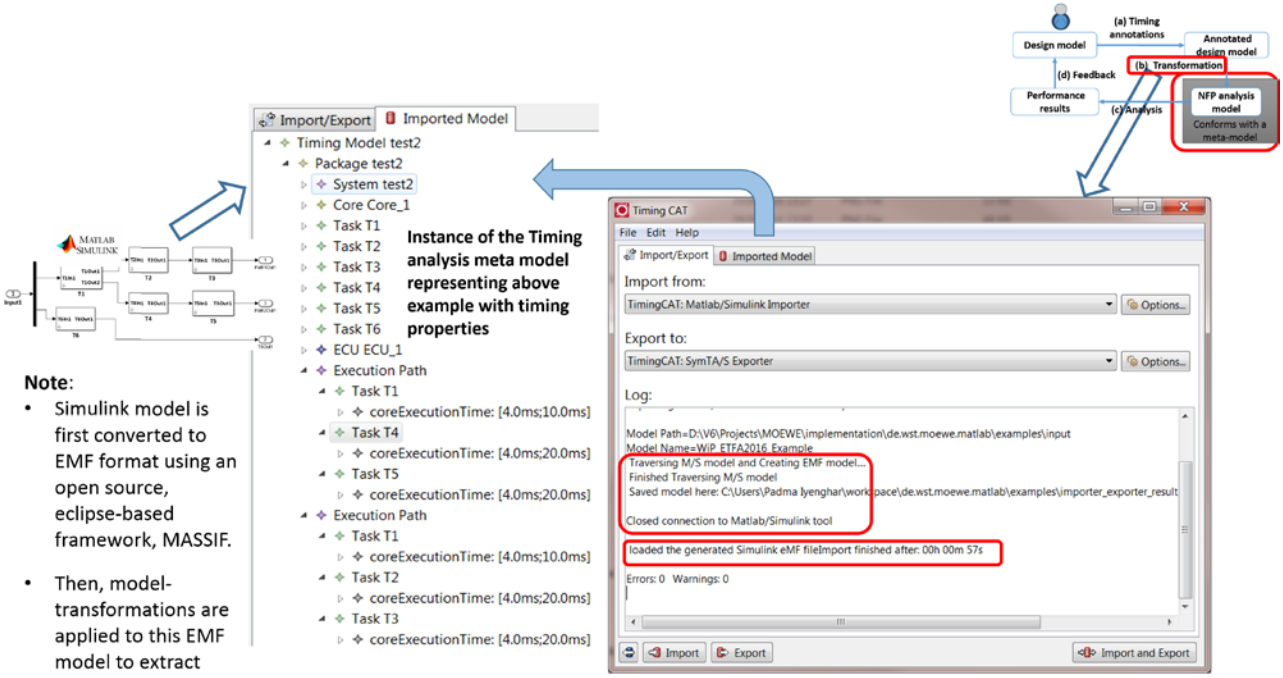
The innovation in the field of embedded systems has been increasingly relying on software-implemented functions. The control laws of these functions typically assume deterministic sampling rates and constant delays from input to output. However, on the target processors, the execution times of the software will depend on many factors such as the amount of interferences from other tasks, resulting in varying delays from sensing to actuating. Three approaches supported by tools, namely TrueTime, T-Res, and SimEvents, have been developed to facilitate the evaluation of how timing latencies affect control performance. However, these approaches support the simulation of control algorithms, but not their actual implementation. The solution to this problem is one of the topics of our on-going research on timing aware model based design (Cyber Physical Action Language CPAL) to automotive applications [1]. In the latest release, timing annotations such as process activation jitters, execution time are included in CPAL.

The purpose of the Short-Term Scientific Mission (STSM) COST-STSM-IC1202-35020 was to experiment and validate those timing features. This eventually resulted in timing analysis of model interpretation engine running in a co-simulation environment considering the run-time delays into account to study the stability of the system.



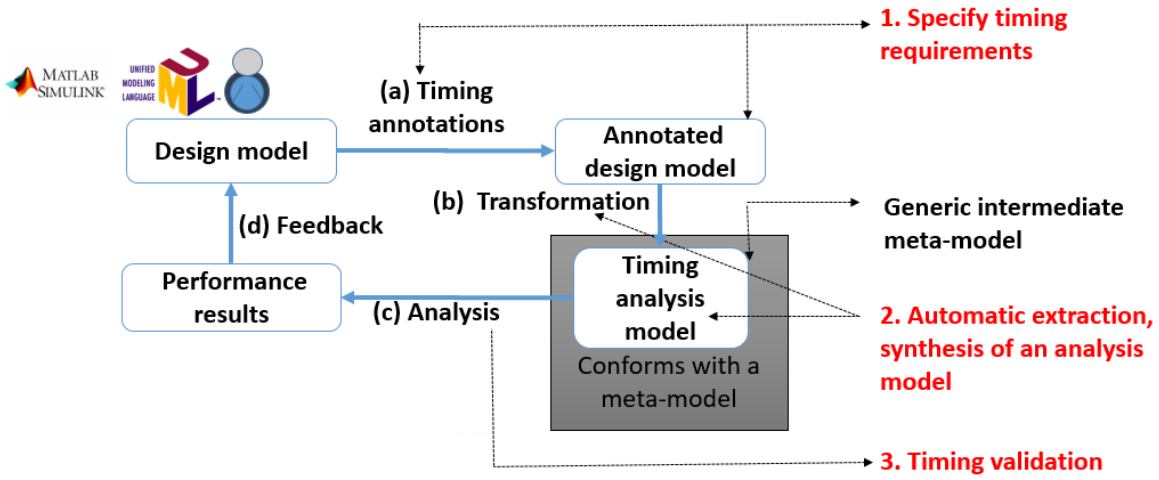
In a control-system simulation, the controller model controls the plant model. In our proposed co-simulation approach a controller model is designed in CPAL, and the plant model is designed in MATLAB/Simulink (MLSL). Controllers can easily be designed in Simulink too. But Simulink is not offering the possibilities to study the behavior of control loops subject to scheduling and networking delays. Varying execution times, preemption delays, blocking delays, kernel overheads cannot be captured in the standard Simulink environment. In order to apply more realistic timing annotations to simulation, it is apparent to get proper timing model of the overall system.

From the earlier discussions [2] and literature [3] we understand that UOS [4] has developed "Timing CAT" a timing analysis meta-model (similar to AMALTHEA timing model) in collaboration with other industry partners. The reason to take UOS timing model in the place of AMALTHEA is we wanted an automated tool (AMALTHEA needs manual efforts) which extracts the timing annotated functional model of the system designed in MLSL (+CPAL).



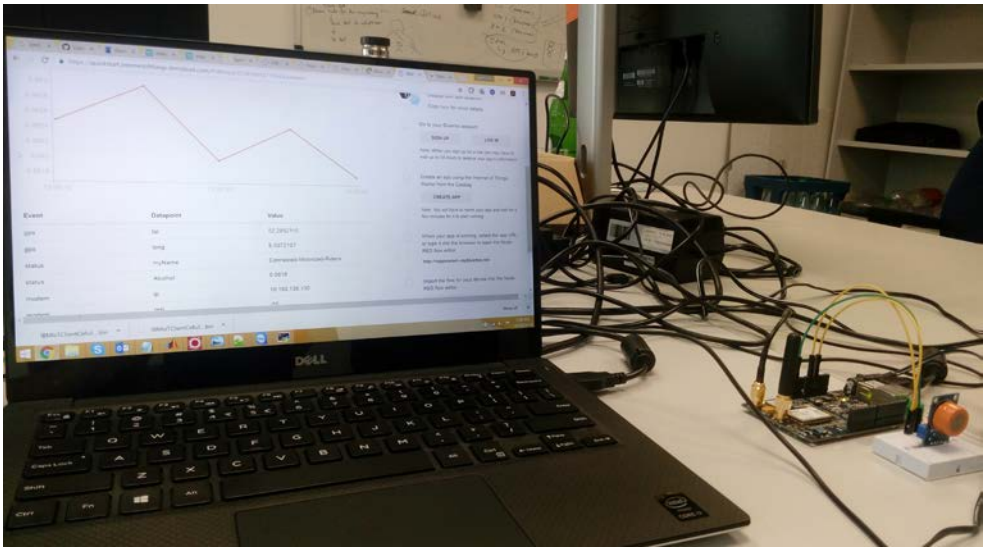
During the first week of stay knowledge sharing of Uni.lux and UOS are done. Subsequently, in the next week, with the help of exchange of information, using Timing CAT, timing model extraction of co-simulation functional model is carried out. This enables early stage timing analysis to improve the design phase.

Towards the third week of the stay, we had set-up a case study "Internet of Things (IoT) enabled smart mobility". (Which is submitted to Grand Challenge 2016 at ISED 2016 [5], selected for finals and achieves the 4 pages of proceeding publication). State of the art practices to IoT development does not consider timing aware model driven methods. Due to this reason, we had set up an IoT experiment which will be used in our on-going research. The experiment is set up with FRDM K64F compatible ARM Cortex M4 board with inbuilt GPS / cellular functionality. Three different cloud platforms are evaluated in the experiment. The application is planned to develop as a high level model (all three options are open - CPAL, MLSL, UML) with timing definitions and low level drivers will be re-used from ARM library.



During the stay we discussed for further collaborative work in this direction which will be impacted soon as one or two potential publications in the line of timing aware model driven development to IoT applications. Writing of conference paper is in progress and will be submitted in December 2016 (aimed for special session on real time aspects of industrial cyber physical systems at ICIT 2017 [6]).

During last (i.e.) third week, PhD co-supervisor Dr Sebastian Altmeyer also participated in some of our meetings when he was a day visit to UOS. UOS also shown interest towards to participate our existing resource aware computing community.



References:

1. FNR - AFR Research project - http://www.fnr.lu/projects/timing-aware-model-based-design-with-application-to-automotive-embedded-systems-2/

2. UOS – Inst. of computer Science – Software Engineering Research Group - University of Osnabruck

3. Related research work at UOS – https://sites.google.com/site/piyengha/publications

4. P. Iyenghar, A. Noyer, J. Engelhardt, E. Pulvermueller, C. Westerkamp: End-to-end path delay estimation in embedded software involving heterogeneous models, 11th IEEE International Symposium on Industrial Embedded Systems (SIES) 2016, Krakow, Poland

5. 6th International Symposium on Embedded computing & system Design (ISED 2016) http://www.ised2016.org/

6. 18th Annual International Conference on Industrial Technology – Special session on real-time aspects of cyber physical systems http://icit2017.org/special-sessions/
