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Short Term Scientific Mission
COST Action IC1202

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Scientific Report

Purpose of the STSM

In hard real-time multitasking systems, all tasks have to provably meet their deadline under any circumstances. In preemptive systems, higher priority tasks may preempt lower priority tasks, thus increasing their worst-case response time (WCRT). When using cached memory, these preemptions may cause additional timing delays when the preempting task evicts instructions or data of the preempted task from cache. WCET analysis can account for these delays, however the analysis results are currently not accounted for in WCET oriented compiler optimizations or optimizations are computationally infeasible.

During the STSM challenges, possible solutions and future collaboration on this topic were discussed.

Work Carried out during the STSM

The STSM took place from 2014/09/08 till 2014/09/12.

At 2014/09/08, both the guest and the host research group gave an overview of their current and future research and discussed possible tie-ins.

From 2014/09/09 till 2014/09/11 a concept was elaborated to connect the current work in the field of test generation by Prof. Abhik Roychoudhury's team with the work on schedulability oriented code optimizations by the applicant.

The STSM ended with a wrap-up meeting on 2014/09/12 in which future collaboration and publications based on the elaborated concept were discussed.

Main Results

A framework to integrate the current work on test generation by the host institution with the WCET focused compiler optimization techniques by the applicant was laid out.
The framework has two important parts: The test generation and the repair.

- Test Generation: The key idea is to use static analysis to find performance stressing test inputs which lead to bad timing behavior. This part of the framework would be similar to [RTSS2013] with changes in the assertion formulation to adapt the analysis to micro-architectural components other than caches.
- Repair: This part will make use of the applicant's WCET focused code optimization techniques as proposed in [JRWRTC2014]. This techniques will be adjusted such that scenarios leading to bad timing behavior are fixed without causing additional bad scenarios by inflicting negative side effects to previously good program paths.

Future Collaboration With Host Institution

For future collaboration, both institutions agreed on sharing their infrastructure to allow for the mutual integration of both institutions' current and future research.

As a direct result of the STSM, the framework which was outlined above will be implemented in the applicant's infrastructure

Foreseen Publications

It is expected, that the implementation and evaluation of the proposed framework will lead to at least one major publication.

Depending on the impact of this framework, additional publications on this topic are expected.

Bibliography

RTSS2013: Abhijeet Banerjee, Sudipta Chattopadhyay and Abhik Roychoudhury, Static Analysis driven Cache Performance Testing,In Proceedings of RTSS. 2013
JRWRTC2014: Arno Luppold and Heiko Falk, Schedulability-Oriented WCET-Optimization of Hard Real-Time Multitasking Systems,In Proceedings of JRWRTC. 2014